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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/850,195	05/08/2001	Radhika Thekkath	MTEC-008/00US	9739
22903	7590	05/10/2005	EXAMINER	
COOLEY GODWARD LLP ATTN: PATENT GROUP 11951 FREEDOM DRIVE, SUITE 1700 ONE FREEDOM SQUARE- RESTON TOWN CENTER RESTON, VA 20190-5061			BADERMAN, SCOTT T	
			ART UNIT	PAPER NUMBER
			2113	
DATE MAILED: 05/10/2005				

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/850,195

Applicant(s)

THEKKATH ET AL.

Examiner

Scott T. Baderman

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 08 May 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-34 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-34 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 08 May 2001 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Drawings

1. Figure 3 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

3. Claims 1-34 are rejected under 35 U.S.C. 102(a) as being anticipated by MIPS Technologies (EJTAG Specification – Document Number MD00047) (hereinafter "MIPS").

As in claim 1, MIPS discloses a test access port comprising: a fastdata register that is selectably connectable to a data register to form at least a portion of a TDI-to-TDO path, said

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fastdata register configured to operate such that a fastdata access completes when a processor access is pending and said processor access is to a predetermined area of dmseg memory (pp. 73-100).

As in claim 2, MIPS discloses a data register serially coupled to said fastdata register (pp. 73-100).

As in claim 3, MIPS discloses wherein said fastdata register is configured to operate such that an attempt to complete said fastdata access occurs by clearing said fastdata register (pp. 73-100).

As in claim 4, MIPS discloses wherein said fastdata register is configured to operate such that said fastdata register is set to indicate that said fastdata access will complete (pp. 73-100).

As in claim 5, MIPS discloses wherein said fastdata register is configured to operate such that, if said processor access is not pending, said fastdata register is cleared to indicate that said fastdata access will not complete (pp. 73-100).

As in claim 6, MIPS discloses wherein said fastdata register is configured to operate such that, if a PrAcc bit is asserted while said processor access is not pending, said fastdata register is cleared to indicate that said fastdata access will not complete (pp. 73-100).

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As in claim 7, MIPS discloses wherein said fastdata register is configured to operate such that, if said processor access is outside said predetermined area of dmseg memory, said fastdata register is cleared to indicate that said fastdata access will not complete (pp. 73-100).

As in claim 8, MIPS discloses a method for transferring a plurality of data words between a test probe and a target processor over a serial link, the method comprising: directing the target processor to configure a test data in port to test data out port ("TDI-to-TDO") path to include a data register and a fastdata register; without reconfiguring said TDI-to-TDO path, shifting each of the plurality of data words accompanied by a SPrAcc bit into said data register and said fastdata register of said TDI-to-TDO path, respectively, said SPrAcc bit indicative of a request for completion of a pending processor access (pp. 73-100).

As in claim 9, MIPS discloses receiving an indication from said TDI-to-TDO path whether said pending processor access completed (pp. 73-100).

As in claim 10, MIPS discloses wherein said receiving an indication comprises receiving an indication that said pending processor access successfully completed when a processor access was pending at a time of said request and said processor access was to a predetermined area of a dmseg memory (pp. 73-100).

As in claim 11, MIPS discloses wherein said receiving an indication comprises receiving an indication that said pending processor access failed to complete when a processor access was not pending at a time of said request (pp. 73-100).

As in claim 12, MIPS discloses wherein said receiving an indication comprises receiving an indication that said pending processor access failed to complete when a processor access was outside a predetermined area of dmseg memory (pp. 73-100).

As in claim 13, MIPS discloses a method for transferring a plurality of data words between a test probe and a target processor over a serial link, the method comprising: configuring a test data in port to test data out port ("TDI-to-TDO") path to include a data register and a fastdata register; receiving from the test probe one of the plurality of data words accompanied by an SPrAcc bit in said data register and said fastdata register of said TDI-to-TDO path, respectively, said SPrAcc bit indicating a request for completion of a pending processor access; and indicating to the test probe whether said pending processor access completed (pp. 73-100).

As in claim 14, MIPS discloses wherein said indicating comprises indicating to the test probe that said pending processor access successfully completed when a processor access was pending at a time of said request and said processor access was to a fastdata area of a dmseg memory (pp. 73-100).

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As in claim 15, MIPS discloses wherein said indicating comprises indicating to the test probe that said pending processor access failed to complete when a processor access was not pending at a time of said request (pp. 73-100).

As in claim 16, MIPS discloses wherein said indicating comprises indicating to the test probe that said pending processor access failed to complete when a processor access was outside a fastdata area of a dmseg memory (pp. 73-100).

As in claim 17, MIPS discloses stalling on an attempt to access a fastdata area of dmseg memory (pp. 73-100).

As in claim 18, MIPS discloses a method for transferring a plurality of data words between a test probe and a target processor over a link, the method comprising: requesting a serial data transfer; receiving control information in said serial data transfer, said control information indicative of a request for completion of a processor access; and confirming said processor access is pending and a target address associated with said processor access falls within a predetermined acceptable range of memory addresses (pp. 73-100).

As in claim 19, MIPS discloses enabling said serial data transfer upon successfully confirming said processor access is pending and said target address associated with said processor access falls within a predetermined acceptable range of memory addresses for one of said plurality of data words (pp. 73-100).

As in claim 20, MIPS discloses wherein said confirming said processor access is pending comprises detecting a value of a control bit (pp. 73-100).

As in claim 21, MIPS discloses resetting said value of said control bit after successfully confirming said processor access is pending (pp. 73-100).

As in claim 22, MIPS discloses wherein said confirming said processor access is pending and a target address associated with said processor access falls within a predetermined acceptable range of memory addresses is achieved without use of the probe (pp. 73-100).

As in claim 23, MIPS discloses wherein said control information is modified to indicate success or failure of confirming said processor access is pending and a target address associated with said processor access falls within a predetermined acceptable range of memory addresses for said one of said plurality of data words (pp. 73-100).

As in claim 24, MIPS discloses wherein said resetting said value of said control bit is achieved without use of the probe (pp. 73-100).

As in claim 25, MIPS discloses in response to direction from the probe, configuring a test-data-in-port to test-data-out-port ("TDI-to-TDO") path to include a data register and a Fastdata register; and without reconfiguring said TDI-to-TDO path, shifting each of said

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plurality of data words accompanied by said control information in modified or unmodified form over said TDI-to-TDO path and the link (pp. 73-100).

As in claim 26, MIPS discloses wherein said control information is an SPrAcc bit associated with each of said plurality of data words (pp. 73-100).

As in claim 27, MIPS discloses wherein said configuring TDI-to-TDO path to include a data register and a Fastdata register is achieved in response to receiving a FASTDATA instruction from the probe (pp. 73-100).

As in claim 28, MIPS discloses a computer-readable medium comprising a programmable device described in software, the programmable device including a test access port comprising: a Fastdata register that is selectably connectable to a data register to form at least a portion of a test-data-in-port to test-data-out-port path, said Fastdata register configured to operate such that a fastdata access completes when a processor access is pending and said processor access is to a predetermined area of memory (pp. 73-100).

As in claim 29, MIPS discloses wherein the programmable device is a microprocessor core (pp. 73-100).

As in claim 30, MIPS discloses a method for transferring a plurality of data words between a test probe and a target processor over a link, the method comprising: in response to a

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request from the target processor for a serial data transfer, including control information in said serial data transfer, said control information indicative of a request for completion of a processor access; and receiving second control information that confirms said processor access was pending and a target address associated with said processor access falls within a predetermined acceptable range of memory addresses (pp. 73-100).

As in claim 31, MIPS discloses directing that target processor to configure a test-data-in-port to test-data-out-pod ("TDI-to-TDO") path to include a data register and a Fastdata register; and shifting each of said plurality of data words accompanied by said control information in modified or unmodified form over said TDI-to-TDO path and the link (pp. 73-100).

As in claim 32, MIPS discloses wherein said control information is an SPrAcc bit associated with each of said plurality of data words shifted into said TDI-to-TDO path and the link (pp. 73-100).

As in claim 33, MIPS discloses wherein said second control information is an SPrAcc bit associated with each of said plurality of data words shifted out of said TDI-to-TDO path (pp. 73-100).

As in claim 34, MIPS discloses wherein said directing the target processor to configure a TDI-to-TDO path to include a data register and a Fastdata register is achieved by sending a FASTDATA instruction (pp. 73-100).

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Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

See Form PTO-892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott T. Baderman whose telephone number is (571) 272-3644.

The examiner can normally be reached on Monday-Friday, 6:45 AM-4:15 PM, first Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Scott T Baderman
Primary Examiner
Art Unit 2113

STB